Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of forming an oxidized tantalum nitride hard-mask for dual damascene processing, comprising:
providing a semiconductor wafer, said wafer comprising:
a base dielectric layer;
a cap layer overlying the base dielectric layer;
a dielectric layer overlying the cap layer;
one or more hardmask layer overlying the dielectric layer; and
a tantalum nitride layer overlying the hardmask layers;
subjecting the tantalum nitride layer to an oxidation process to convert said tantalum nitride layer to oxidized tantalum nitride (TaO_xN_x).

[c2] A method according to claim 1, wherein the base dielectric layer includes planarized circuit elements to which an electrical connection is to be made.

[c3] A method according to claim 1, wherein the dielectric layer is a single dielectric.

[c4] A method according to claim 1, wherein the dielectric layer is a hybrid dielectric.

[c5] A method according to claim 1, wherein the dielectric layer is a hybrid dielectric.

[c6] A method according to claim 1, wherein the oxidation process is a combined thermal and plasma oxidation process.

[c7] A method according to claim 1, further comprising creating a patterned photoresist layer and etching the tantalum nitride layer prior to oxidation.

[c8] A method according to claim 1, further comprising creating a patterned photoresist layer and etching the oxidized tantalum nitride layer after the oxidation process.

[c9] A dual-damascene method of processing a semiconductor wafer, comprising:
providing a semiconductor wafer having a base dielectric layer, said base dielectric layer having circuit elements embedded therein and planarized flush with the surface thereof to which a subsequent electrical connection is to be made;
forming a cap layer over the base dielectric layer and circuit elements;
forming a dielectric layer over the cap layer;
forming a first hardmask layer (HM1) over the dielectric layer;

forming a second hardmask layer (HM2) over the first hardmask layer;
forming a tantalum nitride layer over the second hardmask layer;
lithographically etching the tantalum nitride layer to form trench openings therein; and
subjecting the etched tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer.

[c10] A method according to claim 9, wherein the dielectric layer is a single dielectric layer.

[c11] A method according to claim 9, wherein the dielectric layer is a hybrid dielectric layer.

[c12] A method according to claim 9 wherein the oxidation process is a thermal and plasma oxidation process.

[c13] A method according to claim 12 wherein the oxidation process further comprises:
providing an oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr;
providing a wafer substrate temperature between 250 degrees C and 400 degrees C; and
providing a plasma power between 250Watts and 1000Watts.

[c14] A dual-damascene method of processing a semiconductor wafer, comprising:
providing a semiconductor wafer having a base dielectric layer, said base dielectric layer having circuit elements embedded therein and planarized flush with the surface thereof to which a subsequent electrical connection is to be made;
forming a cap layer over the base dielectric layer and circuit elements;
forming a dielectric layer over the cap layer;
forming a first hardmask layer (HM1) over the dielectric layer;
forming a second hardmask layer (HM2) over the first hardmask layer;
forming a tantalum nitride layer over the second hardmask layer;
subjecting the tantalum nitride layer to an oxidation process to form an oxidized tantalum nitride layer; and
lithographically etching the oxidized tantalum nitride layer to form trench openings therein.

[c15] A method according to claim 14, wherein the dielectric layer is a single dielectric layer.

[c16] A method according to claim 14, wherein the dielectric layer is a hybrid dielectric layer.

[c17] A method according to claim 14, wherein the oxidation process is a thermal and plasma oxidation process.

[c18] A method according to claim 17, wherein the oxidation process comprises:
providing an oxidation environment with a N_2O flow rate between 500 and 5000 sccm at a chamber pressure between 1 and 10 Torr;
providing a wafer substrate temperature between 250 degrees C and 400 degrees C; and
providing a plasma power between 250Watts and 1000Watts.